allowed if rewritten to be in independent form so that Claim 6 would include all of the limitations of Claims 5, 3, and 1; Claim 9 would include al of the limitations of Claims 5, 3, and 1; Claim 11 would include al of the limitations of Claims 5, 3, and 1; Claim 12 would include al of the limitations of Claims 5, 3, and 1; Claim 16 would include al of the limitations of Claims 5, 3, and 1; and Claim 19 would include al of the limitations of Claims 18, 4, and 2. However, as ultimate base Claims 1 and 2 are clearly allowable over the references applied, the rejection of base Claims 1 and 2 is traversed below.

IMPROPER INTERPRETATION OF ARGUMENTS

The outstanding Action has not properly interpreted Applicants arguments presented in the previous response (filed March 20, 2001) that were directed to the teachings of Agari and to the combined teachings of Agari and Chen and not to those of Chen alone. In this regard, the previous response included no argument that "the Chen teaching refers to an upper wiring line" as incorrectly asserted at the start of the "CONCLUSION" paragraph on page 2 of the outstanding Action. For the convenience of the examiner, the relevant portions of this previous response that are believed to have been improperly interpreted are repeated as follows:

> Turning to the outstanding rejection of Claim 1 under 35 U.S.C. §103 as unpatentable over Iwamatsu in view of Agari and Chen, it is first noted that the Action in effect acknowledges that Iwamatsu does not teach the "determining a layout pattern" specified in Claim 1 as a layout pattern of an MOS transistor formed on an SOI layer that will "satisfy the conditional expression $R \cdot C \cdot f < 1$ where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and f = the operating frequency of said predetermined clock, and $f \geq 500$ MHZ." To whatever extent the device of Iwamatsu has a body region and a fixed potential transmission path extending between it to a body contact, there is no way to know the resistance of this transmission path, the gate capacitance of the MOS transistor, much less that the claimed value of R (the resistance of the fixed potential transmission path extending from the body contact to the body region) · C(the gate

capacitance of the MOS transistor over the body region on a gate oxide film) · f (apparently 2.5 GHz) is less than 1. In order to suggest that the artisan would have made R C f (f≥ 500MHz) less than 1, the Action relies upon the teachings of Agari and Chen.

In this respect, the Action first looks to Agari and asserts that it teaches designing a semiconductor device in a manner "minimizing RC delay from the resistance value and the capacitance value at each wiring part" (see the bottom of page 2 of the Action). Chen is then said to teach doping "the body of an SOI MOS transistor [to] minimize the RC time constant due to the body link." Even if these teachings of Agari and Chen are used to modify the apparent method used to make the device of Iwamatsu, they at best teach including a step of determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec.

While the teaching of "determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines" was referred to, it was as being "taught by Agari," not as being taught by Chen. Likewise, while it was noted that there was reliance in the previous Action on an asserted teaching in Agari of designing a semiconductor device in a manner "minimizing RC delay from the resistance value and the capacitance value at each wiring part," this is not a statement involving Chen.

Moreover, the Chen teachings actually treated here deal with the assertion in the previous Action as to Chen teaching doping "the body of an SOI MOS transistor [to] minimize the RC time constant due to the body link" and to the result of this teaching that would be "a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec." Whatever else can be said of these statements involving Chen, it cannot be reasonably said that they suggest that "the Chen teaching refers to an upper wiring line" as urged in the outstanding Action.

Additional discussion of the Agari taught "wiring part" appears in the paragraph

bridging pages 3 and 4 of the last response. This paragraph does not even mention Chen, such that it cannot reasonably be the basis for the improper conclusion in the outstanding Action that Applicants argued "that the Chen teaching refers to an upper wiring line." Once again, the relevant discussion of the previous response that has not been properly interpreted in the outstanding Action is repeated here as follows:

> The Action appears to suggest (at the top of page 3) that Agari somehow teaches minimizes [sic, minimizing] the RC time constant of a body contact because of the improperly extracted reference to a "wiring part" at the bottom of page 2 of the Action. However, it is clear that Agari actually teaches the optimizing of wiring line widths and spacings in terms of minimizing the RC delay of a "wiring part," where the term "wiring" is one the artisan would not use to describe a body contact portion. Thus, when the "PURPOSE" and all of the "CONSTITUTION" portions of the "ABSTRACT" are read together to understand what Agari is referring to as a "wiring part" and the typical use of the term "wiring" is considered, it is clear that line width and spacing are relative to standard surface wiring and this width and spacing of the "wiring part" are controlled to minimize RC delay by controlling values of resistance and capacitance corresponding thereto. In this last regard, it is well established to be "impermissible within the framework of section 103 to pick and choose from any one reference only so much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art" (In re Wesslau, 147 USPQ 391, 393 (CCPA 1965)).

ARGUMENTS HAVE BEEN IMPROPERLY TAKEN OUT OF CONTEXT

In addition to misconstruing arguments in the previous response that clearly were directed to Agari's teachings as being arguments directed to Chen's teachings, the outstanding Action has improperly taken these and other arguments out of context and twisted the associated meaning.

In this respect, Applicants did not argue "that recessed region 20 'is not concerned' with region 32 of the Chen device" as asserted at the bottom of page 2 of the outstanding Action. Instead, the actual argument at the middle of page 4 of the last response was that "[w]hile Chen further refers to the RC time constant of a region 20 in Fig. 1, this RC time

constant is not at all concerned with region 32 illustrated in Fig. 1 of Chen" (emphasis added).

In this regard, Chen states that controlling the RC time constant "in the body link or recessed region 20" involves providing an "appropriate doping concentration in recessed region 20" at col. 7 lines 29-33. As Chen notes at col. 3, lines 10-18, the mesas 24 containing the channels 32 are surrounded by these recessed regions 20. Chen then notes (at col. 3, lines 19-22) the transistors formed on the mesas 24 have a body and that these bodies are in ohmic contact with each other because of the recessed region 20 of silicon layer 18. Col. 3, lines 22-25, next make the nature and extent of the recessed region 20 clear by stating that this recessed region 20 "may be formed by thermal oxidation of silicon layer 18 in a selected pattern which results in a layer of field oxide 38 thereover." Thus, Chen clearly differentiates the transistor channels 32 in mesas 24 from the recessed regions 20 under field oxide layer 38 that surround these mesas as well as distinguishing the recessed regions 20 under field oxide layer 38 from the remaining transistor body portions.

Consequently, when Chen states (at col. 7 lines 29-33) that controlling the RC time constant "in the body link or recessed region 20" involves providing an "appropriate doping concentration in recessed region 20," the nature of what Chen has defined to be the recessed region 20 "underneath field oxide 38" cannot be ignored. Just as the nature of the body link or recessed region 20 cannot be ignored, the description of channels 32 as part of mesas 24 that are connected to substrate contact 39 by the recessed region 20 also cannot be ignored. In this respect, even col. 7, lines 31-32 note that recessed region 20 extends "from a respective channel to substrate contact 39," not that it includes any of the a respective channels 32 or the substrate contact 39.

Similarly, applicants did not argue "that the RC time constant of concern to Chen et al. may not derive from the capacitance of the MOS transistor and the resistance of the

transmission path" as asserted at the top of page 3 of the outstanding Action. Instead, applicants pointed out (in the paragraph bridging pages 3 and 4 of the last response) the lack of any evidence presented by the PTO that demonstrates that any of Chen, Iwamatsu, or Agari teaches "any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region the and multiplying the result by a clock frequency f that is equal to or greater than 500 MHZ and insuring that the final result is greater than one" (emphasis added).

IMPROPER REFERENCE INTERPRETATION

Besides not accurately reflecting the actual argument made, the last noted improper paraphrasing of the actual argument ignores its most important aspect as to the lack of any teaching or suggestion in any of Chen, Iwamatsu, or Agari to use gate capacitance for the C suggested at col. 7, lines 29-33 of Chen. Thus, while this portion of Chen teaches that "[w]ith appropriate doping concentration in recessed region 20, the RC time constant in the body link or recessed region 20 from a respective channel to substrate contact 39 can be as short as or less than 1 nsec," it is "the RC time constant in the body link or recessed region 20" that is referenced not the gate capacitance claimed. The manner in which Chen defines the recessed region 20 as surrounding mesas 24 and being under field oxide layer 38 is fully discussed above. This Chen definition clearly precludes the attempt in this and the last action to create a disclosure in Chen that the gate capacitance is some how reasonably involved with "the RC time constant in the body link or recessed region 20."

In this last respect, it is further clear that Chen does not mention gate capacitance. On the other hand, Chen recites (in col. 1, lines 20-22) the advantages of SOI structures as

including "less junction capacitance so higher circuit speed can be achieved." Moreover, Chen describes (in col. 3, lines 56-60) a doping concentration of the recessed region 20 and the depletion width between the source and/or drain region and the recessed region 20. This description clearly concerns a junction capacitance between the source and/or drain region and the recessed region 20, and it is well known that a capacitance value of such a junction capacitance is highly influenced by the doping concentration of the recessed region 20.

Therefore, it is only reasonable to regard "C," recited in col. 7, lines 29-33 of Chen, as the junction capacitance whose capacitance value is highly influenced by the doping concentration of the recessed region 20, from the technical background wherein

· "C" minimizes the RC time constant to be less than 1, and

· makes the doping concentration of the recessed region 20 an appropriate value.

In this regard, it was and is the burden of the PTO to demonstrate a *prima facie* case of obviousness which means the PTO must show that the relied upon references teach all of the limitations of the claims without resort to speculation to fill gaps missing from reference teachings. Note the following from In re Warner, 154 USPQ 173, 178 (CCPA 1967):

> A rejection based on section 103 clearly must rest on a factual basis, and these facts must be interpreted without hindsight reconstruction of the invention from the prior art. In making this evaluation, all facts must be considered. The Patent Office has the initial duty of supplying the factual basis for its rejection. It may not, because it may doubt that the invention is patentable, resort to speculation, unfounded assumptions or hindsight reconstruction to supply deficiencies in its factual basis. To the extent the Patent Office rulings are so supported, there is no basis for resolving doubts against their correctness. Likewise, we may not resolve doubts in favor of the Patent Office determination when there are deficiencies in the record as to the necessary factual bases supporting its legal conclusion of obviousness. [Emphasis added.]

Instead of pointing to a reasonable basis to interpret this disclosure that "the RC time constant in the body link or recessed region 20" as suggesting that "C" is the claimed gate capacitance, the outstanding Action (top of page 3) mistakenly asserts that "MOS transistor"

capacitance is the only source of "capacitance in the Chen device." This assertion is mistaken because it ignores that the completed device of Chen will have wiring to the source, drain and gate of the transistors of the nature illustrated by FIG. 4, where such wiring has capacitance as taught by Agari. It is further mistaken in ignoring the limitation of concern in Claim 1 requires C to be gate capacitance and not simply some form of stray capacitance or junction capacitance like the junction capacitance noted at col. 1, lines 20-22 of Chen. More importantly, Chen's statement itself ties reducing the RC time constant "in the body link or recessed region 20" to "appropriate doping concentration in recessed region 20."

Thus, it is clear that the PTO improperly attempts to suggest that because Chen does not explain how the "C" portion of the referenced RC time constant arises because of doping in recessed region 20, it can substitute speculation that some form of MOS transistor capacitance is present and that perhaps Chen meant to reference this MOS transistor capacitance instead. Taking its speculation one step further, gate capacitance is then arbitrarily selected from known forms of transistor capacitance because this is what Claim 1 requires and not because of any teaching in the relied upon references. The PTO has violated its initial duty of supplying the factual basis for its rejection and improperly substituted speculation, unfounded assumptions, and hindsight reconstruction. Consequently, the rejection of Claim 1 should be withdrawn for the reasons noted in the previous response as follows:

> In the final analysis, what Claim 1 requires is the use of a layout pattern of an MOS transistor formed on an SOI layer that will "satisfy the conditional expression $R \cdot C \cdot f > 1$ where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and f = the operating frequency of said predetermined clock, and $f \geq 500$ MHZ" (emphasis added). None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a clock frequency f that is equal to or greater than 500 MHZ and insuring that the final result is greater than one.

The rejection of Claim 1 should also be withdrawn for the further reasons noted at page 5 of the previous response, as follows:

> In addition to lacking any evidence that the artisan would have some reason to consider the product of the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed and the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region to be important to control, the Action further lacks any evidence that the artisan would have a prior art based reason to believe that this RC product having an R value and a C value from different elements is somehow a measure of how quickly the signal decays as stated at the top of page 3 of the Action. Similarly lacking is some prior art based reason to believe that this particular RC product having an R value determined by an interior body region and a C value related to a gate electrode over an oxide layer of transistor should be minimized as to a clock signal period so as to produce some desired beneficial result. As noted by In re Sporck, 133 USPQ 360, 364 (CCPA 1962):
>
> > Obviousness is a legal conclusion which we are required to draw from facts appearing in the record or of which judicial notice may be taken. Thus before we can conclude that any disclosed invention is 'obvious' under the conditions specified in 35 U.S.C. 103, we must evaluate facts from which to determine (1) what was shown in the prior art at the time the invention was made, and (2) the knowledge which a person of ordinary skill in the art possessed at the time the invention was made. Here, neither the record nor the facts of which we are able to take judicial notice supplies the factual data necessary to support the legal conclusion of obviousness of the invention at the time it was made. We are unwilling to substitute speculation and hindsight appraisal of the prior art for such factual data.

With respect to Claim 2-5 and 18, the discussion starting at the bottom of page 5 and continuing through the top of page 8 of the previous response is again believed to be relevant and is repeated here for the examiner's convenience as follows:

> Turning to Claim 2, it is again noted that this claim is similar to Claim 1 as to the method of designing that is recited and the semiconductor device to be designed. The differences relate to the requirements of Claim 2 that relate to a signal propagation delay time being provided instead of the Claim 1 operating frequency and the determining of the layout pattern being based on this signal propagation delay time instead of the Claim 1 operating frequency. In this

regard, Claim 2 requires the layout pattern to be determined so that (R·C) / td <1 with the definitions of R and C being the same for Claim 2 as for Claim 1 and "td" being the signal propagation delay time of the MOS transistor which must be less than or equal to 50 ps.

Once again relative to Claim 2, it is believed to be clear that if the artisan where to reasonably use the teachings of Agari and Chen to design the device of Iwamatsu, he would merely add a step as to determining an optimum wiring line width and spacing to result in minimizing RC delay as to the wiring lines shown in the upper portion of Fig. 1 of Iwamatsu as taught by Agari and a separate doping step to dope body links between body contacts and MOS transistors so that these body links themselves have a body link RC time constant as short as or less than 1 nsec. This is not the method set forth by Claim 2.

Similarly, with respect to independent Claim 2, the teachings of Agari cannot be based upon extracting terms out of context and assigning meanings thereto that are not consistent with the meanings clearly used by Agari. See again the Wesslau decision discussed above. The rejection of Claim 2 is also traversed as relying upon an improper interpretation of the language "wiring part" used by Agari just as the rejection of Claim 1 was.

Moreover, and as noted above, even if Agari is assumed to somehow teach minimizing the RC time constant of a body contact, the body contact of Chen is just that, not any of the doped body links disclosed to be between body contacts and MOS transistors also taught by Chen. What Claim 2 requires, on the other hand, is the use of a layout pattern to form an MOS transistor on an SOI layer that will satisfy the conditional expression (R·C) / td > 1 where C = the gate capacitance of said MOS transistor, R = the resistance of a fixed potential transmission path extending from said at least one body contact to said body region, and td = signal propagation delay time required for the MOS transistor, with td being less than or equal to 50 ps. None of Iwamatsu, Agari, or Chen teach any reason at all to consider multiplying the resistance value R of a fixed potential transmission path extending from a body contact to a body region of the nature claimed by the capacitance value C of a gate of an MOS transistor formed on an oxide film over the body region and multiplying the result by a signal propagation delay time td required for the MOS transistor, with td being less than or equal to 50 ps and insuring that the final result is less than one.

Clearly, the resistance "R" of concern in Claim 2 is again that of a "fixed potential transmission path" extending from a body contact to a body region as discussed above and not the resistance of the wiring line of concern to Agari. In addition none of Iwamatsu, Agari, or Chen teach any reason to use the capacitance "C" of the MOS transistor gate electrode along with this value R of an internal transmission path to form an RC product, much less one that meets the Claim 2 requirement that (R·C) / td <1 with td being less than or equal to 50 ps. Once again, valid rejections can only be made if they are based upon

established facts as to the prior art. The rejection of Claim 2 is also traversed because speculation and hindsight based upon applicants' disclosure have again been used as a substitute for facts not of record.

Substantially the same arguments made above as to Claims 1 and 2 apply equally to Claims 3 and 5 which ultimately depend on Claim 1 and Claims 4 and 18 which ultimately depend on Claim 2. In addition, each of these dependent claims add further features to the base claims which are neither taught nor disclosed by the applied references considered alone or in any proper combination. Accordingly, the rejections of Claims 3-5 and 18 are traversed for the reasons presented above as to base Claims 1 and 2 as well as because there has been no establishment of any *prima facie* case of obviousness as to these additional features which are also not taught or suggested by the references relied upon.

Since no other issues are believed to be outstanding in the present application, it is believed to be clearly in condition for formal allowance. Consequently, an early and favorable action to that effect is earnestly and respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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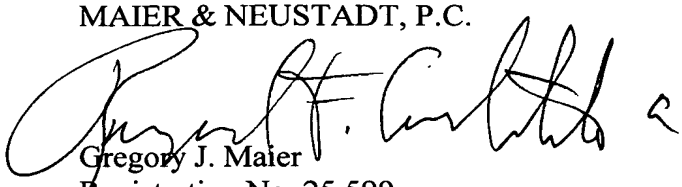

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